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(71) Applicant
Qualcast Garden Products Limited

(Incorporated in United Kingdom)

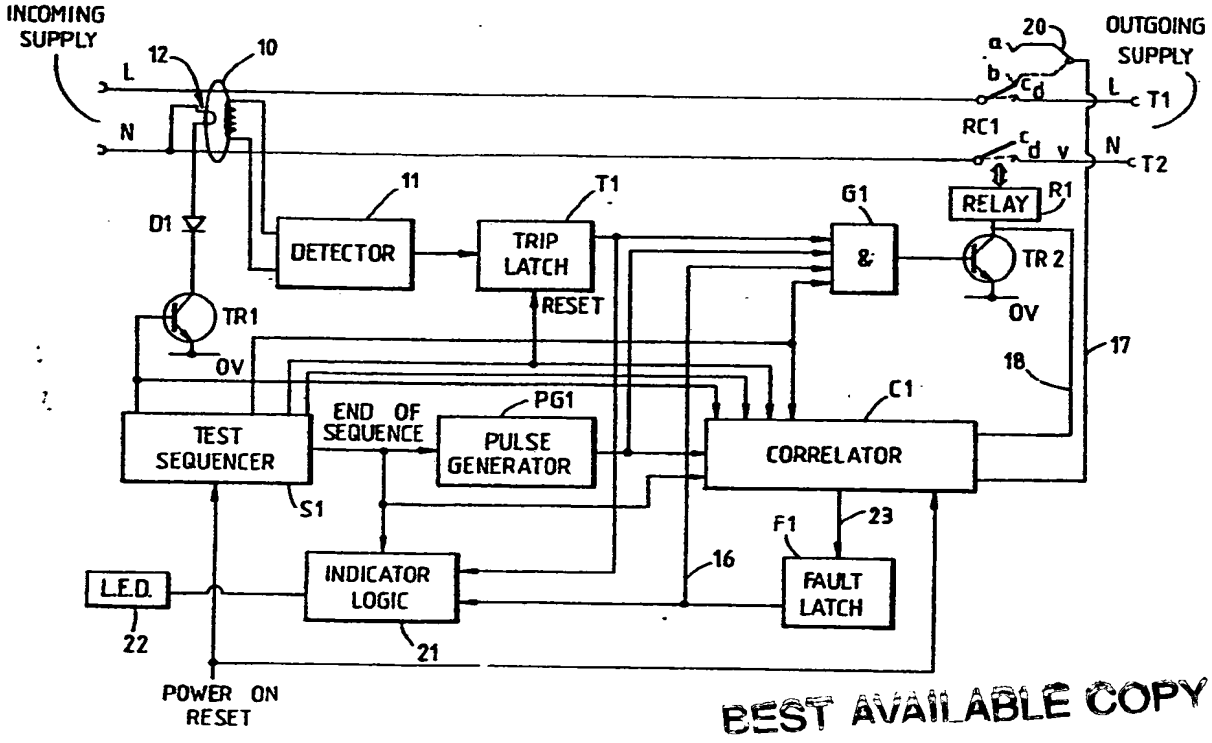
Coleridge Street, Sunnyhill, Derby, DE3 7JT

(72) Inventor
Paul D Ducker

(74) Agent and/or Address for Service
Brookes & Martin
High Holborn House, 52/54 High Holborn,
London, WC1V 6SE

(54) Testing residual current circuit breakers

(57) A residual current circuit breaker (RCD) comprises a pair of conductors L,N for connecting a load to an electric power supply, means 10,11 for sensing when the currents flowing in the respective conductors differ by a predetermined amount, tripping means TR2,R1 responsive to the output of the sensing means for tripping a circuit breaking device RC1 to interrupt the outgoing supply of current to the load, means 12 for introducing a simulated fault or trip signal, means for monitoring the response of at least one circuit component to the simulated signal, and means C1 for correlating the response with the initial application of the signal to provide a pass/fail signal. The arrangement can produce a sequence of tests in response to a power-on signal, and may also apply test pulses continuously during operation without causing disconnection.



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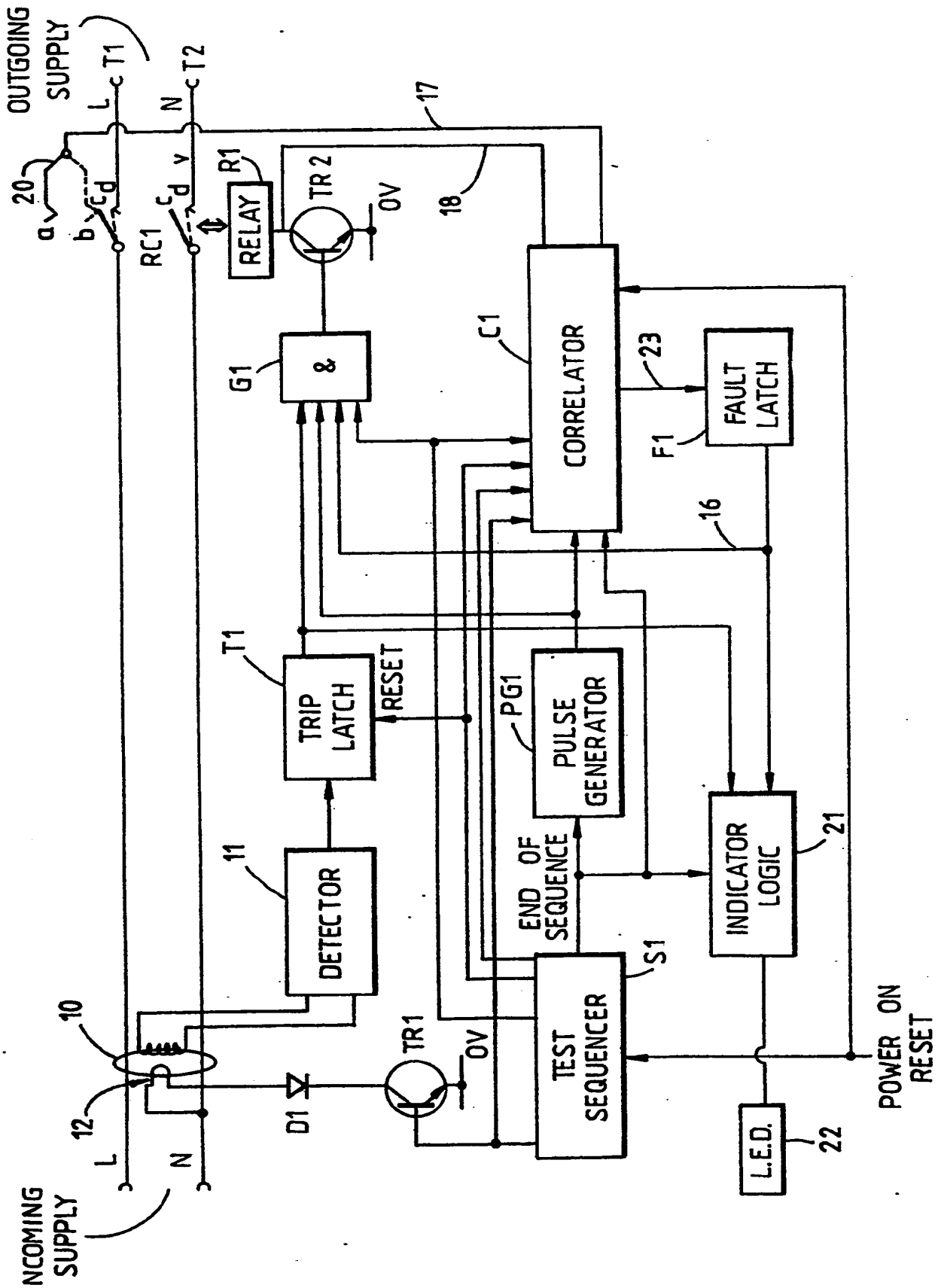

RESIDUAL CURRENT CIRCUIT BREAKERS

A residual current circuit breaker (RCCB or RCD) generally includes means for sensing an imbalance in the currents flowing in the live and neutral supply lines of the appliance to be protected, and means responsive to an output from the sensing means for tripping a circuit breaking device to isolate the outgoing supply terminals. It may also include a test circuit in which a simulated trip current trips the circuit breaker, and means for re-establishing or resetting the circuit breaker to restore the outgoing supply after the test. Such tests are normally initiated and the outcome interpreted by the user via a mechanically related or transmitted function such as a push button.

A particular drawback of this known type of test circuit is its reliance on the user always remembering to perform the test prior to using the RCD. Additionally, even if the test fails, the user may still be tempted to use the RCD to provide an outgoing supply to an electrical appliance.

Additional test circuits have included systems for testing only the fault sensing part of the RCD subsequent to the outgoing supply being established.

According to a first aspect of the present invention there is provided a residual current circuit breaker (RCD) comprising a pair of conductors for connecting a load to an electric power supply, means for sensing when the currents flowing in the respective conductors differ by a predetermined amount, tripping means responsive to the output of the sensing means for

tripping a circuit breaking device to interrupt the outgoing supply of current to the load, means for introducing a simulated fault or trip signal, means for monitoring the response of at least one circuit component to the simulated signal, and means for correlating the response with the initial application of the signal to provide a pass/fail signal.

According to a second aspect of the invention there is provided a residual current circuit breaker (RCD) comprising a pair of conductors for connecting a load to an electric power supply, means for sensing when the currents flowing in the respective conductors differ by a predetermined amount, tripping means responsive to the output of the sensing means and controlling the status of a circuit breaking device for interrupting the outgoing supply, means for injecting pulses of current into the tripping means, means for monitoring the resulting response of the circuit breaking device, the magnitude and/or duration of the pulses being such that the response is monitored either without interrupting the outgoing supply or with the interruptions having a negligible effect on the supply, and means for correlating the injected pulses with the monitored response to provide a pass/fail signal.

In the present specification there is described a RCD with a test circuit in which three test sequences test the ability of the RCD to perform its protective function both before and after connecting a load to the outgoing supply.

In one test sequence, the circuit breaking device is initially set in its non-tripped state representative

of the outgoing supply being established. A simulated fault signal is then introduced and the resulting change of state of the tripping means and/or of the circuit breaking device is detected. The tripping means and/or the circuit breaking device are finally reset only in response to a signal indicating that the said change of state has been detected. The means for initially setting the circuit breaking device to its non-tripped state is preferably operable in response to a signal indicating the absence of a load across the outgoing supply terminals.

A means of isolating the tripping means from the trip sensing detector provides a second test sequence whereby the tripping means is disabled and the response to the simulated fault signal is detected as a change of state at the trip sensing detector. This second sequence is preferably used as a pre-test to the first sequence whereby the trip system is tested without enabling the circuit breaking device.

Only if the tests indicate the tripping means and circuit breaking device are operating satisfactorily is the outgoing supply finally enabled via the circuit breaking device such that a load can be safely operated when connected across the outgoing supply terminals. Thereafter a third sequence may be used as part of the test system whereby test pulses are continuously injected through the tripping means. The magnitude and/or duration of the pulses are so determined that the effects thereof can be monitored at or about the circuit breaking device but either without interrupting the outgoing supply or with interruptions that have a negligible effect on the supply. Each test pulse is then correlated with the

corresponding response, the absence of correlation indicating failure of the tripping means and/or circuit breaking device. A resulting fail signal from the correlator may then attempt to isolate the outgoing supply and/or indicate failure of the RCD during use.

At least part of the test system is preferably an auto-test circuit responsive to a power "on" signal.

By way of example only, a system embodying all three test sequences will now be described with reference to the accompanying drawing in which the sole figure is a schematic circuit diagram of a RCD circuit including an auto-test system embodying the invention.

The illustrated circuit may be housed within an adaptor which is plugged into a mains socket, the circuit having outgoing supply terminals T1, T2 connected to an outgoing supply socket in the adaptor housing for receiving a plug connected to the appliance being protected. Alternatively, the illustrated circuit might be included within the housing of the mains socket itself. In this case an on/off power switch would be included.

The circuit includes a conventional fault sensing mechanism comprising a toroid 10 with a sensing coil which senses a difference in the currents flowing in the live and neutral conductors of the power line, and a detector 11 for detecting an imbalance in the sensed currents. In addition, however, a third conductor 12 passes through the toroid to provide a simulated fault signal to the detector when a transistor TR1 is pulsed "on" by an output from a test sequencer S1.

An output from the detector 11 sets a latch T1 to trip a relay drive transistor TR2 driving a relay R1. In operation the transistor TR2 is normally biased "on" so that the relay R1 is energised and the relay contacts RC1 are pulled in. The relay R1 and relay contacts RC1 form the circuit breaking device so that, when the latch T1 is set in response to an output from the detector 11, the relay is tripped (de-energised) and the contacts RC1 open to isolate the outgoing supply terminals T1, T2.

An auto-test circuit is provided to check the operation of the toroid 10, detector 11, trip latch T1, drive transistor TR2 and relay R1 before enabling the output at terminal T1 and T2 for finally supplying power to the appliance to be protected. The test sequencer S1 starts in response to a power "on" signal. The sequencer S1 then provides a first sequence of signals in which the latch T1 is isolated from the tripping circuit by disabling the output gate G1, and a second sequence of signals in which the gate G1 is enabled, thereby including drive transistor TR2 and relay R1 in the test sequence.

A test interlock is also included via signal line 17 to provide a check for socket vacancy, contact weld and relay open or closed. These checks are performed by detecting electrical contact between the moving contact of the relay RC1 and a floating back contact 20 fixed on the shutter mechanism associated with the outgoing supply socket. The electrical contact, and consequently circuit 17 to a correlator C1, is only made when the relay contacts RC1 are at the relaxed or "outgoing supply interrupted" position "c", and the contact 20 located on the shutter mechanism is at the

position "b" indicating that the socket is vacant. However, when a plug is inserted in the socket, the contact 20 is moved out of the "b" position to the "a" position and is no longer able to complete the electrical circuit 17 to the correlator. Features of this test interlock are further described and separately claimed in our copending application being filed concurrently herewith.

Initially a fault latch F1 is cleared (reset). Each check for continuity of line 17 is then performed at the appropriate time in the test sequence by a pulse from sequencer S1 enabling the input 17 on to the fault latch F1 via the correlator C1 and line 23. If the socket is vacant and the relay R1 is in its relaxed state, the input 17 to the fault latch has no effect. If however the socket is occupied and/or the relay is not relaxed, the fault latch is set via line 17 by the mains related voltage on power line L.

In the first test sequence a check for continuity is initially made on the signal at 17 to ensure that the contacts RC1 are not welded or sticking, and the outgoing socket is vacant. A check is also made via signal line 18 to verify the non-conducting status of the relay drive transistor TR2.

As well as checking for continuity of line 17, the correlator C1 also consists of set/reset latches and co-operates with the sequencer S1 so that when a test is initiated by a pulse from the sequencer at a first count, this sets a latch in the correlator. The consequence of the test should then reset the latch at the next count if the result is valid. If the latch is not reset, the fault latch F1, responsive to a fail

with the short clock pulse signals from the pulse generator such that a latch is set in the correlator by the leading edge of the clock pulse and then reset by the leading edge of the pulse returned on line 18. If at any time the line 18 does not change state prior to the trailing edge of the clock pulse being detected the fault latch F1 is set, the relay R1 disabled and the indicator LED 22 extinguished.

In a preferred method of generating the simulated fault signal, alternate half-wave pulses from a bridge rectifier in the power supply for the RCD are applied to the third conductor 12 through the toroid 10 by connecting the transistor TR1 between a diode D1 and the Ov line of the bridge rectifier, the other side of the diode being connected to the neutral conductor (N) of the power line via the third conductor 12.

CLAIMS

1. A residual current circuit breaker (RCD) comprising a pair of conductors for connecting a load to an electric power supply, means for sensing when the currents flowing in the respective conductors differ by a predetermined amount, tripping means responsive to the output of the sensing means for tripping a circuit breaking device to interrupt the outgoing supply of current to the load, means for introducing a simulated fault or trip signal, means for monitoring the response of at least one circuit component to the simulated signal, and means for correlating the response with the initial application of the signal to provide a pass/fail signal.

2. A RCD according to claim 1 in which the circuit component comprises the tripping means and/or the circuit breaking device.

3. A RCD according to claim 1 or claim 2 wherein the circuit breaking device is tripped and/or the outgoing supply inhibited in response to a fail signal.

4. A RCD according to any one of the preceding claims wherein an interlock preventing the circuit breaking device from supplying outgoing current is removed or disabled in response to a pass signal.

5. A RCD according to any one of the preceding claims further comprising an indicating device having a status responsive to the pass/fail signal.

6. A RCD according to any one of the preceding

claims wherein the correlation is, or forms part of, a sequence of tests which are performed at least partially by electrical means in the form of test circuitry.

7. A RCD according to claim 6 wherein the test or sequence of tests is initiated in response to a power "on" signal.

8. A RCD according to any one of the preceding claims in which the simulated fault or trip signal is introduced by electrically controlled means.

9. A RCD according to any one of the preceding claims further comprising electrically controlled means for setting the circuit breaking device into a conducting state.

10. A RCD according to any one of the preceding claims wherein the sensing means includes detecting means for detecting when a sensed difference in the currents exceeds the predetermined amount.

11. A RCD according to claim 10 wherein a latching circuit is included between the detecting means and the tripping means.

12. A RCD according to claim 6 or claim 7 in which the test sequence includes several correlation functions each correlating the response of a selected component or components to the simulated fault signal and contributing to the outcome of the pass/fail signal.

13. A RCD according to any one of the claims 6, 7

or 12 further comprising means for inhibiting the circuit breaking device from providing an outgoing supply whilst part or all of the test sequence is being performed to establish the pass/fail signal.

14. A RCD according to claim 13 wherein the tripping means includes a latching circuit and a first test sequence correlates the response of the latching circuit to a simulated fault signal whilst the circuit breaking device is disabled.

15. A socket according to claim 14 wherein a second test sequence comprises means for enabling the circuit breaking device after checking for absence of a load across the conductors and a fail signal has not previously been generated, the simulated fault signal being correlated with the response from the latching circuit, tripping means and circuit breaking device to generate a fail signal if the correlation is unsuccessful, and means responsive to the absence of a fail signal for thereafter re-enabling the circuit breaking device after again checking for absence of a load across the conductors.

16. A RCD according to any one of the preceding claims in which the simulated fault or trip signal is provided on a third conductor passing with the said pair of mains conductors through a toroid having a sensing coil.

17. A RCD according to claim 16 in which one end of the third conductor is connected to the neutral mains conductor and the other end is connected via a unidirectional current flow device to the collector of a transistor having its emitter connected to the zero

checking at each stage of the sequence is achieved in the same manner as in the previous tests.

The second sequence terminates after the correlator has again checked for socket vacancy and tripped relay contact status, the sequencer S1 then resetting the trip latch T1 and enabling the output gate G1 to energise the relay R1. A final check is then made on line 17 to confirm that the relay contacts RC1 have pulled in.

At the end of the two stage test sequence indicator control logic 21 is also enabled by an end-of-sequence signal from sequencer S1 which, provided the sequences have been completed without a fault being detected, drives an LED 22 to indicate completion of the auto test sequence. The trip signal from latch T1 is also fed to the indicator logic 21 so that a genuine trip causes the LED 22 to flash.

The end-of-sequence signal also enables a pulse generator PG1 and corresponding logic in the correlator to provide a continuing test system after the initial test sequence has been successfully completed and the outgoing supply has been established.

In this case the pulse generator PG1 supplies short clock pulses each capable of disabling the gate G1 and turning the relay control transistor TR1 off only momentarily. The pulse period is such that the decay of relay current can be detected at the relay control transistor TR2 via signal line 18, but is insufficient to actually cause movement of the relay contacts RC1. The output or return pulse on line 18 is correlated

signal on line 23 indicating the absence of correlation at the next count, is set to disable the gate G1 and thereby prevent the relay R1 subsequently being energised to enable the outgoing supply. The absence of a fail signal on line 23 at the end of a test is effectively treated as a pass signal for that test. Assuming the fault latch has not been set, the first test sequence continues by resetting the trip latch T1, with the gate G1 disabled. A trip signal is next introduced by the sequencer S1 via test transistor TR1, and the correlator C1 checks the trip is detected at the trip latch T1 output.

At the end of the first sequence the correlator again checks for a signal on line 17 corresponding to continued socket vacancy and the relay R1 being at the rest position. The sequencer S1 next resets the trip latch T1 and enables the output gate G1 which in turn energises the relay R1 via transistor TR2 to close the contacts RC1. The correlator then checks the relay contacts RC1 have pulled in by verifying that signal on line 17 has been interrupted, corresponding to the relay contacts moving from position "c" to position "d".

At the beginning of the second sequence the sequencer again injects a pulse to the test transistor TR1 to provide a simulated fault signal, and the sequence continues by correlating the response of the circuit to this fault signal. In particular the correlator checks the trip latch T1 has been set, the relay control transistor TR2 is turned off, and the relay contacts RC1 have returned to the tripped position "c" re-establishing electrical contact with the shutter contact 20 at position "b". The correlation and

voltage line of a bridge rectifier in a power supply.

18. A mains supply socket including a RCD according to any one of the preceding claims and further comprising means for detecting the absence of an electrical plug in the socket and/or the conductive status of the circuit breaking device.

19. A socket according to claim 18 when dependent on claim 6, 7, 12, 13, 14 or 15 wherein an interlock is included in the test sequence to ensure the outgoing supply is not made onto an electrical plug occupying the mains supply socket.

20. A residual current circuit breaker (RCD) comprising a pair of conductors for connecting a load to an electric power supply, means for sensing when the currents flowing in the respective conductors differ by a predetermined amount, tripping means responsive to the output of the sensing means and controlling the status of a circuit breaking device for interrupting the outgoing supply, means for injecting pulses of current into the tripping means, means for monitoring the resulting response of the circuit breaking device, the magnitude and/or duration of the pulses being such that the response is monitored either without interrupting the outgoing supply or with the interruptions having a negligible effect on the supply, and means for correlating the injected pulses with the monitored response to provide a pass/fail signal.

21. A RCD according to claim 20 in which a fail output from the correlator indicating that the tripping means and/or circuit breaking device are

unable to interrupt the outgoing supply enables the tripping means to attempt interruption of the supply and/or activates a fault indicator.

22. A RCD substantially as herein described with reference to the accompanying drawing.

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